[0264] Referring back to FIG. **15**, the controller **720** controls operations of the output units **710-1** and **710-2**. The controller **720** turns on the output units **710-1** and **710-2** in response to an (i−1)-th carry signal CR[i−1] output from an (i−1)-th driving stage. The controller **720** turns off the output units **710-1** and **710-2** in response to an (i+1)-th carry signal CR[i+1] output from an (i+1)-th driving stage. In such an embodiment, the controller **720** maintains the turned-off state of the output units **710-1** and **710-2** according to the switching signal output from the inverter **730**.

[0265] FIG. **16** displays a period HPi (hereinafter referred to as an i-th period) during which the i-th gate signal G[i] has a high level VH-G, the previous period HP(i−1) (referred to as an (i−1)-th period), and the next period HP(i+1) (referred to as an (i+1)-th period), among a plurality of periods.

[0266] The first control transistor T**4** outputs a control signal, which controls a potential of the first node Q, to the first node Q. The second control transistor T**9** provides the second ground voltage VSS**2** to the first node Q in response to the (i+1)-th carry signal CR[i+1] output from the (i+1)-th stage. The third control transistor T**10** provides the second ground voltage VSS**2** to the first node Q in response to a switching signal output from the inverter **730**.

[0267] As shown in FIGS. **15** and **16**, a potential or voltage level of the first node Q (VQ[i] in FIG. **16**) is increased to a first high level VQ**1** by the (i−1)-th carry signal CR[i−1] during an (i−1)-th period HP(i−1).

[0268] During the i-th period HPi, the i-th gate signal G[i] is output. When the i-th gate signal G[i] is output, the first node Q is boosted to a second high level VQ**2** from the first high level VQ**1**.

[0269] During the i-th period HPi, the (i−1)-th carry signal CR[i−1] of the low level VL-C of the previous driving stage is applied to the second control end of the first control transistor T**4**. During the i-th period HPi, an (i+1)-th carry signal CR[i+1] of the low level VL-C of the next driving stage is applied to the second control end of the second control transistor T**9**.

[0270] The i-th carry signal CR[i−1] of the low level VL-C of the previous driving stage and the (i+1)-th carry signal CR[i+1] of the low level VL-C of the next driving stage have voltages that are similar to or equal to the back bias voltage VBB. Therefore, the threshold voltages of the first and second control transistors T**4** and T**9** are increased (i.e., positive-shifted).

[0271] Since the threshold voltages of the first and second control transistors T**4** and T**9** are increased, the first node Q is boosted to the second high level VQ**2**, and thus, even though a voltage difference at lateral ends of the first control transistor T**4** is increased, a leakage current according to the increase of the voltage difference at lateral ends of the first control transistor T**4** is reduced. In such an embodiment, although a voltage difference between lateral ends of the second control transistor T**9** is increased, a leakage current according to the increase of the voltage difference between lateral ends of the second control transistor T**9** is reduced. Accordingly, the potential of the first node Q is maintained at the second high level VQ**2** so that the i-th gate signal G[i] may be output with a sufficiently high level.

[0272] During the i-th period HPi, the i-th carry signal CR[i] is output. In a period excluding the i-th period HPi, the carry signal CR[i] of the low level VL-C is applied to the second control end of the second output transistor T**15**. Then, the threshold voltage of the second output transistor T**15** is increased (i.e., positive-shifted). Thus, a leakage current of the second output transistor T**15** is reduced so that a ripple at the carry terminal CR can be reduced.

[0273] During the (i+1)-th period HP(i+1), the second control transistor T**9** provides the second ground voltage VSS**2** to the first node Q in response to the (i+1)-th carry signal CR[i+1] output from the (i+1)-th stage.

[0274] At the time point t**23** at which the (i+1)-th period HP(i+1) starts, the voltage of the first node Q is reduced to the second ground voltage VSS**2**. Accordingly, the first output transistor T**1** and the second output transistor T**15** are turned off. Until the (i−1)-th gate signal G[i−1] of the next frame period is output after the (i+1)-th period HP(i+1), the voltage of the first node Q is maintained at the second ground voltage VSS**2**. Thus, until the (i−1)-th gate signal G[i-1] of the next frame period is output after the (i+1)-th period HP(i+1), the first output transistor T**1** and the second output transistor T**15** maintain the turned-off state.

[0275] The voltage of the second node A (VA[i] in FIG. **16**) has substantially the same phase as the first clock signal CKV, excluding the i-th period HPi. In a period excluding the i-th period HPi, a ripple generated from the carry terminal CR may be applied to the first control ends of the third and fourth inverter transistors T**13** and T**8**. The second ground voltage VSS**2** is applied to the input ends of the third and fourth inverter transistors T**13** and T**8**. A leakage current may flow through the third and fourth inverter transistors T**13** and T**8** due to a potential difference between the first control ends and the input ends of the third and fourth inverter transistors T**13** and T**8**.

[0276] In such an embodiment, the first clock signal CKV transmitted to the control end of the second inverter transistor T**7** through the first inverter transistor T**12** may be discharged through the third inverter transistor T**13**. Then, the voltage of the second node A has a phase that is different from that of the first clock signal CKV. Accordingly, the third control transistor T**10**, the second holding transistor T**11** and the third holding transistor T**31**, control ends of which are connected to the second node A, may not effectively operate.

[0277] According to an exemplary embodiment, the back bias voltage VBB is applied to the second control ends of the third and fourth inverter transistors T**13** and T**8** to increase the threshold voltages of the third and fourth inverter transistors T**13** and T**8**. Thus, the leakage current of the third and fourth inverter transistors T**13** and T**8** due to the ripple generated at the carry terminal CR may be reduced.

[0278] According to an exemplary embodiment, the input end of the third inverter transistor T**13** is connected to the first ground terminal V**1**. In such an embodiment, a potential difference V_{GS} between the input end and the control end of the third inverter transistor T**13** is reduced to thereby reduce the leakage current of the third inverter transistor T**13** caused by the ripple generated at the carry terminal CR.

[0279] In such an embodiment, during the i-th period HPi, the third and fourth inverter transistors T**13** and T**8** are turned on in response to the i-th carry signal R[i]. When the third and fourth inverter transistors T**13** and T**8** are turned on, the first clock signal CKV of the high level VH-C, output from the second inverter transistor T**7**, is synchronized with the second ground voltage VSS**2** through the fourth inverter transistor T**8**, such that the second ground voltage VSS**2** may be applied to the second node A.